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XICOR X9258T, 9250T

Digital Controlled Potentiometers

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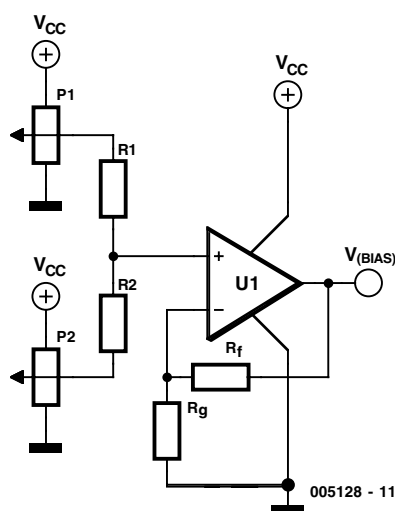


Figure 1. XDCP-based wide range bias driver for RF power amplifiers.

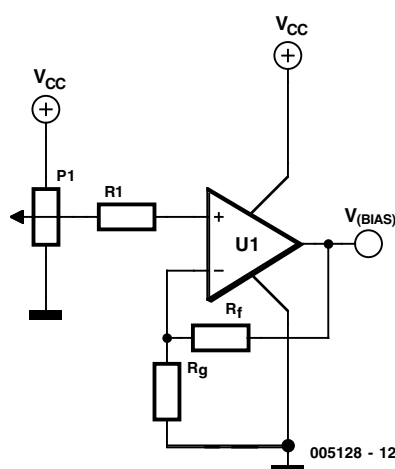


Figure 2. High resolution biasing of LDMOS transistors.

One of the most important aspects of PA design is the biasing network. It is important for the bias network to reject RF power. Using high impedance sources where possible accomplishes this. Where low impedance sources are used, it is imperative to maintain a good decoupling regime, to maximize the transistor's performance.

At the FET drain (GaAs or LDMOS), it is necessary to use a low impedance bias supply. For transistors not biased class A, the current versus output power characteristic is dynamic, and any residual power supply impedance will cause amplitude modulation of the drain voltage.

Most commercial power amplifiers have a bandwidth typically of a maximum 10%, and therefore it is possible to supply drain current using a RF shorted quarter wave section (which will transform to an open circuit at the feed point). For wideband applications (octave plus), it is generally better to use an inductor to feed bias to the drain.

The bias voltage may be fed onto the transistor gate-matching network via a surface mount resistor. Typically, the resistance would be of the order of a few hundred ohms to ensure that minimal RF power leaks through the resistor into the biasing network. As the gate is extremely high impedance and therefore the current requirement is negligible, it is possible to use the smallest package size readily available (typically

0603). This will reduce the effect of any package parasitic resonance, maximizing stability and performance.

For LDMOS applications, thermal compensation would be done using either a simple analogue compensation scheme or using DSP to control the XDCP. The gate voltage change with respect to temperature (for constant drain current) is around -2mV.K^{-1} . Normally, the compensation constant would be a slightly different to this to maintain a constant gain versus temperature response. The biasing (quiescent current) requirement varies between applications, but for a typical SCPA (single carrier power amplifier) a quiescent current tuning resolution of 1% of $I_{d\text{q_opt}}$ is all that is needed. $I_{d\text{q_opt}}$ is the typical bias condition, which offers maximum dynamic gain flatness and almost optimum two-tone third order intermodulation distortion when a device is biased class AB. This is easily achieved using an 8-bit XDCP, X9258T or X9250T with 256 wiper positions.

Application	Resolution
MCPA (Multi Carrier Amplifier)	8-bit or 2 x 6-bit
Large Dynamic Conduction Angle Variation	2 x 6-bit
SCPA (Single Carrier Amplifier)	6-bit or 8-bit

Some applications, for example MCPA (multicarrier power amplifier)

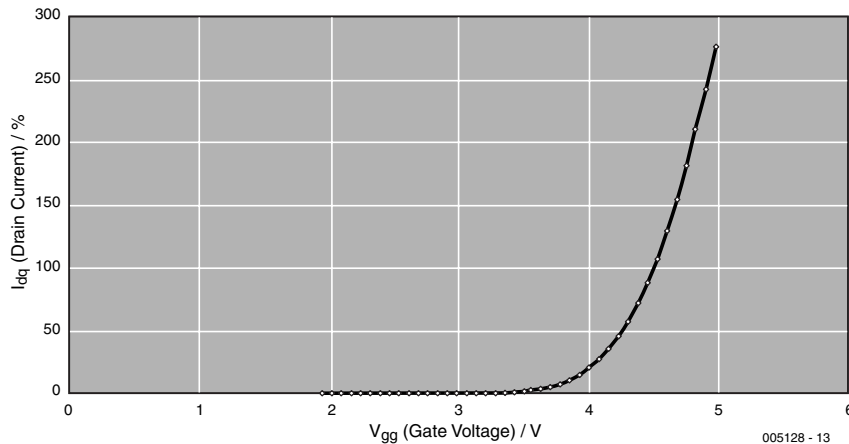


Figure 3. LDMOS DC operating characteristic, drain current (% of I_{dq_opt}) as a function of gate voltage.

may require finer bias control or greater dynamic range to optimize dynamic gain flatness. In some cases, it may be desirable to actually

change the bias class (conduction angle) completely, from A through AB to B and possibly beyond.

As shown in **Figure 1**, this can

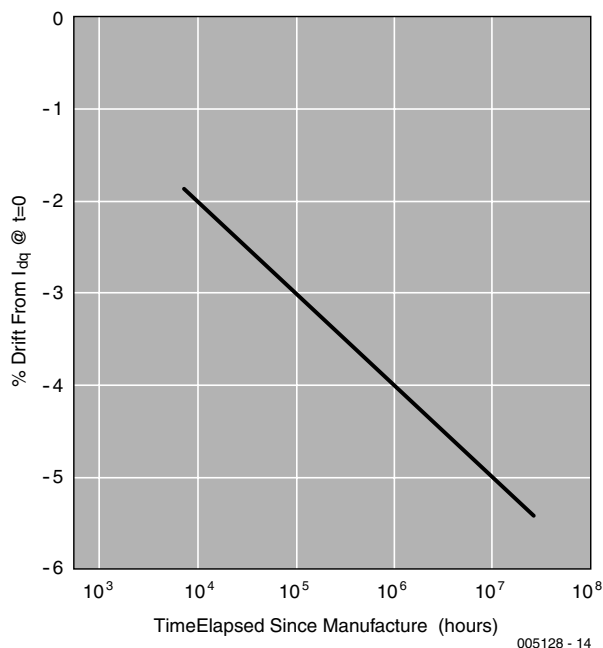


Figure 4. Typical LDMOS drift characteristic.

also be easily achieved using two XDCPs and a weighted summing network at the buffer op-amp input ... effectively doubling the bit resolution. Two combined 6-bit (64 positions) XDCPs can achieve 12-bit (4096 positions) resolution.

By selecting the ratio R1/R2 to be the same as the number of tap points (in this case 6 bits = 64 positions), it is possible to achieve a dividing resolution of more than 4000 wiper positions. This arrangement is more than adequate to provide high resolution biasing of

LDMOS devices, while giving maximum flexibility to bias the transistor in any class of operation.

In the circuit shown in **Figure 2**, The X9250 8-bit potentiometer will generally give the required voltage resolution, especially when the range of voltage outputs is conditioned. This can be done by selecting upper and lower limits for the high and low side of the potentiometer.

Additionally, the op-amp buffer allows further flexibility for range adjustment and the introduction of an offset.

A typical LDMOS transistor requires a change of approximately 2.5mV in gate voltage to effect a 1% change in drain current. (**Figure 3**). It is therefore possible to use a single 8-bit potentiometer to tune over a range of 0.6V with 1% resolution. Using the 2 x 6-bit potentiometer example highlighted earlier, gives the potential for 1% resolution over a 10 V range, though normally the range would be reduced to allow greater resolution.

On-chip memory is another feature incorporated in most of the XDCP range. This allows the designer to load a set of four values for each potentiometer, and dynamically assign the memory register to the potentiometer at any point in time.

Generally, it is not necessary to use these memory settings. The settings would nor-

mally be stored and controlled by an external processor and memory. Reloading new values to the wiper register doesn't result in any spurious noise at the wiper.

This allows the PA bias setting to be dynamically reprogrammed while 'hot' with RF power, with no detrimental (or even detectable) effect.

This is theoretically the worst time possible to change bias conditions on the transistor, as any spikes on the bias supply could result in large amounts of current drawn by the transistor, enhanced by the RF power, with possibly terminal consequences.

The memory settings are most likely to be utilized for many power amplifier design features.

Digital thermal compensation

Thermal conditions are monitored by the system microcontroller. This can use a look-up table or algorithm to calculate the best operating point for the transistor. A preset list of discrete values can be loaded into the memory at production time, and loaded into the wiper register when necessary.

V_g/I_d drift compensation

LDMOS transistors suffer from performance drift over time. The net effect is that a slightly increased amount of gate voltage is required to maintain a given drain current. LDMOS processes are being refined continually, and current drift figures are typically 5% over 20 years. Most of this drift occurs while the

amplifier is undergoing test in the factory; effectively burning the device in, before delivery. Drift is also proportional to the process cut-off frequency. A typical drift characteristic is shown in **Figure 4**.

Other RF Applications – An Example

The XDCP can be used in a wide variety of other RF applications. A good example would be the vector modulator.

The purpose of the vector modulator is to manipulate an arbitrary signal, allowing its amplitude and phase to be varied in a controlled manner. Recently, it has become a popular method for complex gain adjustment in linearized amplifier systems, both feed forward and predistortion.

The vector modulator consists of a 3dB 90-degree hybrid, an in-phase combiner, and two variable attenuators, realised either with a pair of mixers or two further 3-dB 90-degree hybrids with diodes. Analysis of the vector modulator is straightforward, and is not detailed here.

The advantages of using a XDCP over a DAC are the same as for the power amplifier application. The vector modulator example serves only to highlight another of the

numerous applications where significant benefit can be derived.

Summary

The XDCP offers the reliability and flexibility of the DAC for the cost of the mechanical potentiometer, giving the designer the rare opportunity to make a win-win design improvement.

The new software interface allows easy prototyping of a dynamic programming environment with a minimum of hardware.

Flexibility of the XDCP is such that it may also be used in the PA periphery and control circuitry, not only for biasing of transistors. Additionally, it may supersede the use of the DAC in other cost critical RF sub-systems.

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Xicor XDCP devices are available through Kanda Systems Ltd., Unit 17-18, Glanrafon Enterprise Park, Aberystwyth, Ceredigion SY23 3JQ, United Kingdom. Tel. (01970) 621030, fax (01970) 621040.

Email sales@kanda.com, website <http://www.kanda.com>

CORRECTIONS&UPDATES

537 'Lite' Computer January & February 2000, 990054

The chip select lines address the following memory ranges:

CS0\	E000 - E7FF
CS1\	E800 - EFFF
CS2\	F000 - F7FF
LCD	F800 - FFFF

8-bit I/O Port July/August 2000, 994077

Due to logic level contention, this interface can only operate as an 8-bit input or an 8-bit output. Using the PCF8574 to monitor input logic levels on K4 will

result in driver logic reflections on K5. Conversely if using the PCF8574 to drive the output of K5, the dc logic level on K4 will adversely affect the correct operation of the PCF8574.

EEDTS Pro Super Loco Decoder October 1999, 990071

The circuit of the decoder programmer, Figure 5, contains two transistors 'T2'. One of these should be labelled 'T3'. The correct type numbers of T2 and T3 are BD680, not BD560 as shown. The value of C4 should be 2.2nF, not 1 nF as shown.

HotKeys Keyboard (1 & 2) April & May 2000, 002006

If hard to find locally, the 8-MHz ceramic resonator for this project may be replaced by a quartz crystal. The crystal wires are then connected to the outer two holes originally provided for the resonator. Two 27pF capacitors are connected between the crystal wires and the central solder pad.

The parts list in part 2 of the article contains an error. The correct type number of the caps for S1-S16 is 707023-01.

3-Volts Car Adapter July/August 2000, 000014

A capacitor (C2) of 100nF (0.1 μ F) should be fitted between R2 and ground.

PIC17C Processor Board September 2000, 000061

Contrary to what is stated in the Components List, the -A version of the PIC processor is suitable for use in this circuit. The PIC17C756A is a 'shrink-wrap' version of the 'C756'. The standard PIC17C756 is no longer produced.